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Attorney Docket No.: 021653-001500US
Title: Method and Structure of Manufacturing High Capacitance Metal on Insulator Capacitors in Copper
Applicant: Xian Jie Ning
Replacement Drawing Sheet 1 of 3

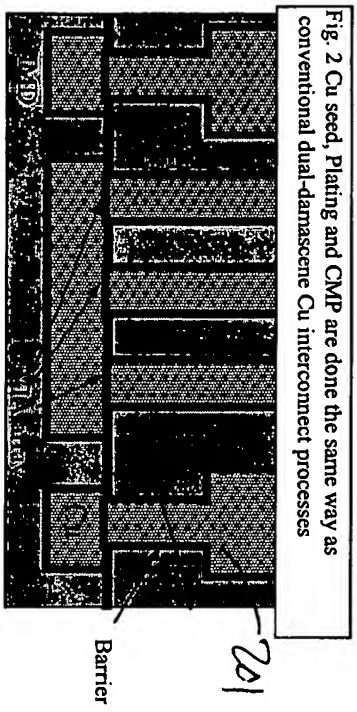

Fig. 2 Cu seed, Plating and CMP are done the same way as conventional dual-damascene Cu interconnect processes

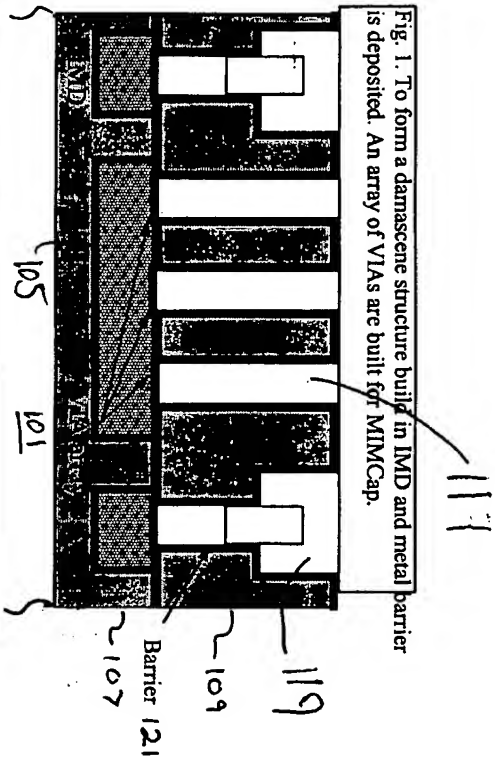

Fig. 1. To form a damascene structure build in IMD and metal barrier is deposited. An array of VIAs are built for MIMCap.

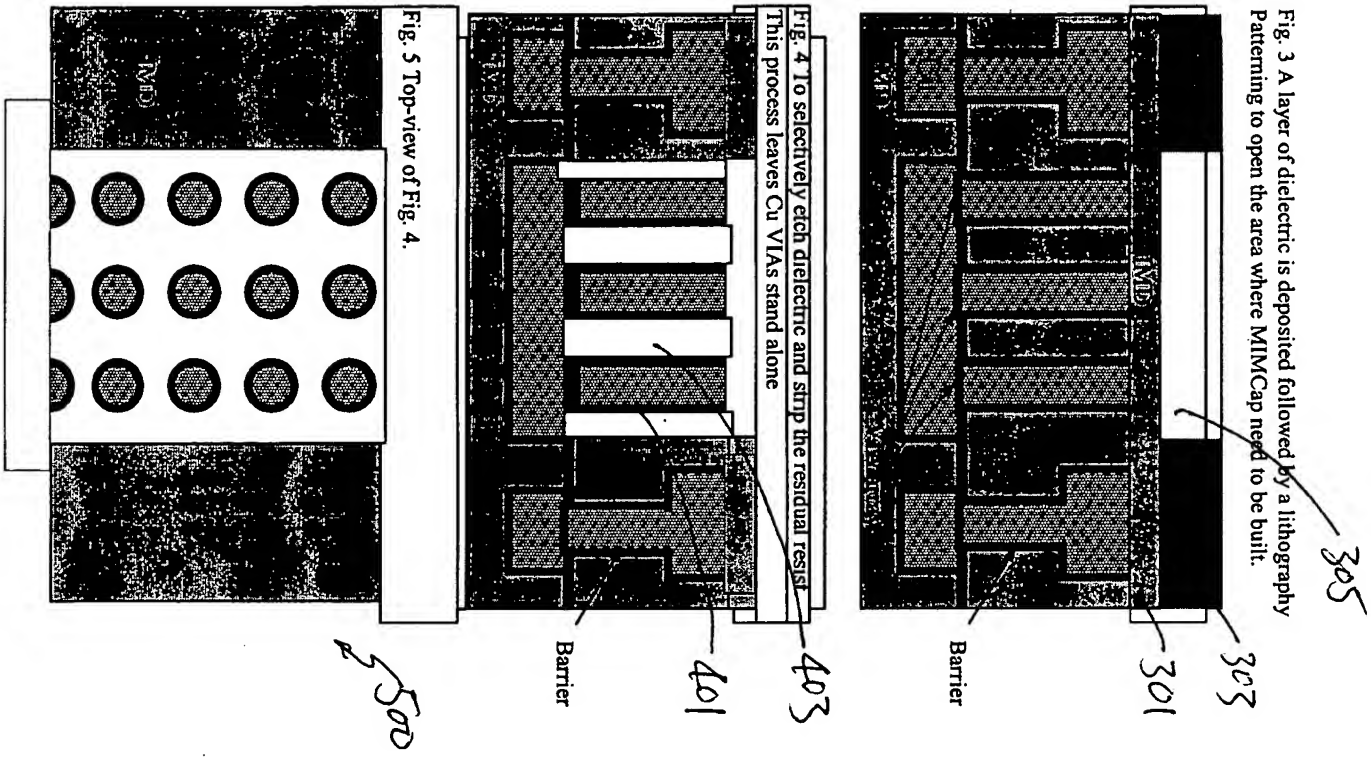

Fig. 3 A layer of dielectric is deposited followed by a lithography Patterning to open the area where MIMCap need to be built.

Fig. 4 To selectively etch dielectric and strip the residual resist This process leaves Cu VIAs stand alone

Fig. 5 Top-view of Fig. 4.

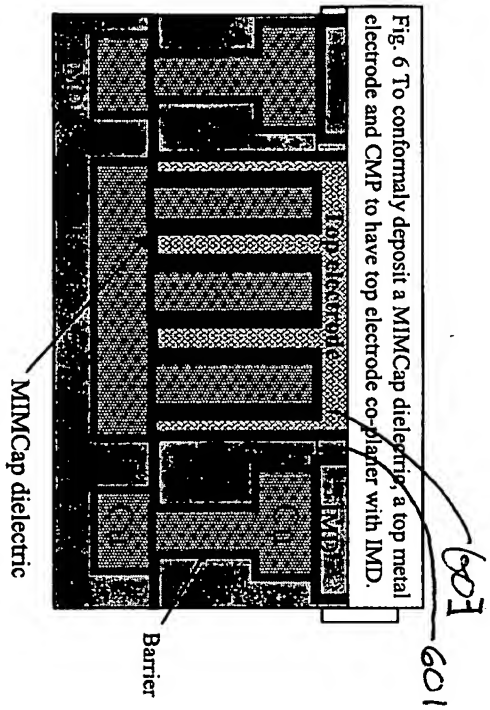

Fig. 6 To conformaly deposit a MIMCap dielectric, a top metal electrode and CMP to have top electrode co-planer with IMD.